Module Code	**EEU44C02**
Module Name	Microelectronic Circuits
ECTS Weighting[2]	5 ECTS
Semester taught	Semester 2
Module Coordinator/s	Adjunct Prof. Phillip Christie
Module Learning Outcomes with reference to the Graduate Attributes and how they are developed in discipline	This module will provide students with an understanding of the of how the Very Large Scale Integration (VLSI) of digital circuits containing billions of transistors is achieved. The structure of the module is split into two parts: a theoretical component which addresses how complex non-linear pehenomena that underly both transistor and interconnect operation can be efficiently modelled, and a software tool component which describes the algorithms which underly Electronic Design Automation (EDA). Theory is allocated two lectures per week and covers the physics of MOS transistors devices with a focus on non-ideal transistor behaviour, models for circuit and wire delays, and mathematical models of the complexity of VLSI circuits. The software tool component covers Electronic Design Autmation (EDA) tool flows and is based on a combintation of six lectures and three labs. LO 1: Model and simulate the performance of large VLSI systems at the device, circuit and system levels LO 2: Predict whether a given VLSI circuit can be successfully routed with a given number of wiring layers in a specified foundry technology. LO 3: Understand how Electronic Design Automation (EDA) tools work together to create a physical layout of a VLSI circuit. **Graduate Attributes: levels of attainment** To act responsibly - Enhanced To think independently - Enhanced To develop continuously - Enhanced To communicate effectively - Enhanced

Module Content

Please provide a brief overview of the module of no more than 350 words written so that someone outside of your discipline will understand it.

- ***The MOSFET:*** incorporation of the device equations governing transistor operation into device models using VerilogA which is used in circuit simulators (such as SPICE). Incorporation into the VerilogA models of the non-ideal effects encountered in highly-scaled MOS devices.
- ***Circuit simulation***: use of device models to characterise large numbers (100s) of digital logic blocks using a library charecterisation tool.
- ***Synthesis***: How to translate the HDL functional description of a circuit into a standard cell netlist using a synthesis tool.
- ***Place and route***: How to optimise the placement of standard cell netlist and the routing of the wires between them using a place and route tool.
- ***Static Timing Analysis***: How to estimate the performance of digitall circuits using a Static Timing Analysis (STA) tool.

Teaching and Learning Methods

This module is taught using a combination of lectures (two lectures per week on VLSI circuits and one lecture per week on VLSI systems), and two supporting three-hour laboratories.

Assessment Details[3]
Please include the following:

- **Assessment Component**
- **Assessment description**
- **Learning Outcome(s) addressed**
- **% of total**
- **Assessment due date**

Assessment Component	Assessment Description	LO Addressed	% of total	Week due
Written Exam	Written Exam		80	End of Semester
Laboratory	Laboratory		20	During Semester

Reassessment Requirements

Supplemental Written Exam

Contact Hours and Indicative Student Workload[3]

Contact hours:
36 hours
Independent Study (preparation for course and review of materials):
35

	Independent Study (preparation for assessment, incl. completion of assessment): 40
Recommended Reading List	Physical Design Essentials, Khosrow Golshan, Springer, 2007. CMOS VLSI Design: a circuits and systems perspective, 4th ed., Neil Weste and David Harris, Pearson Addison Wesley, 2011. Device Electronics for Integrated Circuits, Richard Muller and Theodore Kamins, John Wiley, 2003.
Module Pre-requisite	EEU33C02 Digital Circuits or equivalent, EEU33C07 Digital Systems Design or equivalent
Module Co-requisite	
Module Website	See Blackboard
Are other Schools/Departments involved in the delivery of this module? If yes, please provide details.	No
Module Approval Date	
Approved by	
Academic Start Year	
Academic Year of Date	September 2023