Module Code	EE5M01
Module Name	INTEGRATED SYSTEMS DESIGN
ECTS Weighting[2]	5 ECTS
Semester taught	Semester 1
Module Coordinator/s	Shreejith Shanker
Module Learning Outcomes with reference to the Graduate Attributes and how they are developed in discipline	On successful completion of this module, students should be able to: 1. Build a synchronous DSP system in Verilog and verify its performance. 2. Build and test complex FSMs in Verilog. 3. Automate testbenches for automatic pass/fail. 4. Analyse finite precision effects in digital filters. 5. Make design decisions for fixed point implementations given constraints. 6. Analyse memory usage/requirements for FPGA realisations. 7. Target sequential designs to FPGA hardware. **Graduate Attributes: levels of attainment** To act responsibly - Enhanced To think independently - Enhanced To develop continuously - Enhanced To communicate effectively - Enhanced
Module Content	This module builds directly on the 3C7 Digital Systems Design module from the Junior Sophister year. It will introduce more advanced topics in Verilog-based FPGA design. The approach will be from a systems perspective, looking at the implication of design trade-offs for integrated digital systems typical in DSP and consumer applications. • Finite state machines with data path. • Verilog HDL language. • Automation of test benches and design of golden vectors. • Code coverage. • Finite precision effects and choice of bit-width in fixed-point applications. • Translating DSP systems designed in MATLAB onto an FPGA.

[1] An Introduction to Module Design from AISHE provides a great deal of information on designing and re-designing modules.
[2] TEP Glossary

	• Memory on FPGAs. • Working with FPGA board peripherals. • Realisation of the above concepts in hardware designs.
Teaching and Learning Methods	This is a highly practical module. There will be two “classic” style lectures as well as a two-hour practical session each week which will be a lecture/laboratory slot. The FPGA board used to support the practical sessions is the Xilinx PYNQ-Z2 board. The practical sessions will require the students to complete **3 or 4** assignments outside class hours (average 4 hours extra per week), spreading the load through the year. It is critical that the student keeps up with the practical work during the semester. The formal written two-hour end-of-year examination will contribute 50% of the overall subject mark at the annual and supplemental examination sessions. Practical work from the module will also contribute 50% towards the overall grade. Attendance at weekly practical sessions is compulsory. No marks will be given for the corresponding assignment for unattended practical sessions. **Associated Laboratory/Project Programme** Four 2 hour laboratories will be used to support the existing practical element of the module. There will be no extra assignments from these sessions.

Assessment Details[3] **Please include the following:** • **Assessment Component** • **Assessment description** • **Learning Outcome(s) addressed** • **% of total** • **Assessment due date**	<table><tr><td>Assessment Component</td><td>Assessment Description</td><td>LO Addressed</td><td>% of total</td><td>Week due</td></tr><tr><td>CONTINUOUS ASSESSMENT</td><td>FPGA design lab</td><td>1,2,7</td><td>50</td><td>Announced in the labs</td></tr><tr><td>Written Exam</td><td>End of year exams</td><td>2,4,5,6</td><td>50</td><td></td></tr><tr><td></td><td></td><td></td><td></td><td></td></tr><tr><td></td><td></td><td></td><td></td><td></td></tr></table>
Reassessment Requirements	100% based on Exam
Contact Hours and Indicative Student Workload[3]	**Contact hours:** 44 (22 hour lectures, 22 hour labs) **Independent Study (preparation for course and review of materials):** 2 hour / week for lecture review/self study [24] **Independent Study (preparation for assessment, incl. completion of assessment):** 2 hours lab prep (formative) [44]
Recommended Reading List	• *Contemporary Logic Design*, 2nd edition, Randy H Katz, University of California, Berkeley, Gaetano Borriello, University of Washington. • *Digital Design*, 4th edition, MM Mano and MD Ciletti, Digital Design, (Pearson) Prentice Hall, 2007, can be used if it was purchased in the second year but be aware that the examples are in VHDL, not in Verilog. • *Verilog HDL*, 2nd edition, Palnitkar (reference only). • *FPGA Prototyping By Verilog Examples: Xilinx Spartan-3 Version*, Pong P Chu, Wiley (reference only). • *Exploring Zynq MPSoC with PYNQ*, Louise Crockett et.al. (reference, online copy)

[3] TEP Guidelines on Workload and Assessment

Module Pre-requisite	EE3C7 or equivalent
Module Co-requisite	
Module Website	On Blackboard
Are other Schools/Departments involved in the delivery of this module? If yes, please provide details.	
Module Approval Date	
Approved by	
Academic Start Year	September 2023
Academic Year of Date	2024/2025